Hi-performance Regulator IC Series for PCs
Main Power Supply ICs for Note PC (Linear Regulator Integrated)

BD9528MUV

● Description
BD9528MUV is a 2ch switching regulator controller with high output current which can achieve low output voltage (1.0V～5.5V) from a wide input voltage range (5.5V～28V). High efficiency for the switching regulator can be realized by utilizing an external N-MOSFET power transistor. A new technology called H3RegTM (High speed, High efficiency, High performance) is a Rohm proprietary control method to realize ultra high transient response against load change. SLLM (Simple Light Load Mode) technology is also integrated to improve efficiency in light load mode, providing high efficiency over a wide load range. For protection and ease of use, 2ch LDO (5V/100mA, 3.3V/100mA), the soft start function, variable frequency function, short circuit protection function with timer latch, over voltage protection, and Power good function are all built in. This switching regulator is specially designed for Main Power Supply of laptop PC.

● Features
1) 2ch H3REG™ DC/DC Converter controller
2) Adjustable Simple Light Load Mode (SLLM), Quiet Light Load Mode (QLLM) and Forced continuous Mode
3) Thermal Shut Down (TSD), Under Voltage LockOut (UVLO), Over Current Protection (OCP),
   Over Voltage Protection (OVP), Short circuit protection with 0.75ms timer-latch (SCP)
4) Soft start function to minimize rush current during startup
5) Switching Frequency Variable (f=200kHz～500kHz)
6) Built-in Power good circuit
7) Built-in 2ch Linear regulator (5V/100mA, 3.3V/100mA)
8) Built in reference voltage (0.7V)
9) VQFN032x5050 package
10) Built-in BOOT-Di
11) Built-in output discharge

● Applications
Laptop PC, Desktop PC, LCD-TV, Digital Components
### Absolute maximum ratings \((Ta=25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Terminal Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN, CTL, SW1, SW2</td>
<td></td>
<td>30 (^{+2})</td>
<td>V</td>
</tr>
<tr>
<td>EN1, EN2, PGOOD1, PGOOD2</td>
<td></td>
<td>6 (^{+2})</td>
<td>V</td>
</tr>
<tr>
<td>Vo1, Vo2, MCTL1, MCTL2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FS1, FS2, FB1, FB2, ILIM1, ILIM2, SS1, SS2, LG1, LG2, REF, REG2</td>
<td></td>
<td>REG1+0.3 (^{-1})</td>
<td>V</td>
</tr>
<tr>
<td>BOOT1, BOOT2</td>
<td></td>
<td>35 (^{+2})</td>
<td>V</td>
</tr>
<tr>
<td>BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2</td>
<td></td>
<td>7 (^{+2})</td>
<td>V</td>
</tr>
<tr>
<td>HG1</td>
<td></td>
<td>BOOT1+0.3 (^{-2})</td>
<td>V</td>
</tr>
<tr>
<td>HG2</td>
<td></td>
<td>BOOT2+0.3 (^{-2})</td>
<td>V</td>
</tr>
<tr>
<td>PGND1, PGND2</td>
<td></td>
<td>AGND (\pm 0.3) (^{+2})</td>
<td>V</td>
</tr>
<tr>
<td>Power Dissipation1</td>
<td>(Pd1)</td>
<td>0.38 (^{+3})</td>
<td>W</td>
</tr>
<tr>
<td>Power Dissipation2</td>
<td>(Pd2)</td>
<td>0.88 (^{+4})</td>
<td>W</td>
</tr>
<tr>
<td>Power Dissipation3</td>
<td>(Pd3)</td>
<td>3.26 (^{+5})</td>
<td>W</td>
</tr>
<tr>
<td>Power Dissipation4</td>
<td>(Pd4)</td>
<td>4.56 (^{+6})</td>
<td>W</td>
</tr>
<tr>
<td>Operating temperature Range</td>
<td>(\text{Topr})</td>
<td>-20(^\circ)C to +100(^\circ)C</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature Range</td>
<td>(\text{Tstg})</td>
<td>-55(^\circ)C to +150(^\circ)C</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>(\text{Tjmax})</td>
<td>+150(^\circ)C</td>
<td>°C</td>
</tr>
</tbody>
</table>

*1 Do not however exceed \(Pd\).
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 3.0mW for each increase in \(Ta\) of 1°C over 25°C (when don’t mounted on a heat radiation board )
*4 Reduced by 7.0mW for increase in \(Ta\) of 1°C over 25°C. (when mounted on a board 74.2mm \(\times\) 74.2mm \(\times\) 1.6mm Glass-epoxy PCB which has 1 layer. (Copper foil area : 20.2mm\(^2\))
*5 Reduced by 26.1mW for increase in \(Ta\) of 1°C over 25°C. (when mounted on a board 74.2mm \(\times\) 74.2mm \(\times\) 1.6mm Glass-epoxy PCB which has 4 layers. (1st and 4th copper foil area : 20.2mm\(^2\), 2nd and 3rd copper foil area : 5505mm\(^2\))
*6 Reduced by 36.5mW for increase in \(Ta\) of 1°C over 25°C. (when mounted on a board 74.2mm \(\times\) 74.2mm \(\times\) 1.6mm Glass-epoxy PCB which has 4 layers. (All copper foil area : 5905mm\(^2\))

### Operating conditions \((Ta=25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Terminal Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>(\text{VIN})</td>
<td>5.5</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>CTL</td>
<td>(\text{CTL})</td>
<td>-0.3</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>EN1, EN2, MCTL1, MCTL2</td>
<td></td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>BOOT1, BOOT2</td>
<td></td>
<td>4.5</td>
<td>33</td>
<td>V</td>
</tr>
<tr>
<td>SW1, SW2</td>
<td></td>
<td>-0.3</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2</td>
<td></td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Vo1, Vo2, PGOOD1, PGOOD2</td>
<td></td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>MIN ON TIME</td>
<td>(\text{TONmin})</td>
<td>-</td>
<td>150</td>
<td>nsec</td>
</tr>
</tbody>
</table>

★ This product should not be used in a radioactive environment.
### Electrical characteristics

(Unless otherwise noted, Ta=25°C, VIN=12V, CTL=OPEN, EN1=EN2=5V, FS1=FS2=51kΩ)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN standby current</td>
<td>ISTB</td>
<td>70 150 250</td>
<td>μA</td>
<td>CTL=5V, EN1=EN2=0V</td>
</tr>
<tr>
<td>VIN bias current</td>
<td>IIN</td>
<td>60 130 230</td>
<td>μA</td>
<td>Vo1=5V</td>
</tr>
<tr>
<td>VIN shut down mode current</td>
<td>ISHD</td>
<td>6 12 18</td>
<td>μA</td>
<td>CTL=0V</td>
</tr>
<tr>
<td>CTL Low Voltage</td>
<td>VCTLL</td>
<td>-0.3 - 0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CTL High Voltage</td>
<td>VCTLH</td>
<td>2.3 - 28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CTL bias current</td>
<td>ICTL</td>
<td>-18 -12 -6</td>
<td>μA</td>
<td>CTL=0V</td>
</tr>
<tr>
<td>EN Low Voltage</td>
<td>VENL</td>
<td>-0.3 - 0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN High Voltage</td>
<td>VENH</td>
<td>2.3 - 5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN bias current</td>
<td>IEN</td>
<td>- 3 6</td>
<td>μA</td>
<td>EN=3V</td>
</tr>
</tbody>
</table>

#### [5V linear regulator](VIN)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>REG1 output voltage</td>
<td>VREG1</td>
<td>4.90 5.00 5.10</td>
<td>V</td>
<td>IREG1=1mA</td>
</tr>
<tr>
<td>Maximum current</td>
<td>IREG1</td>
<td>100 - -</td>
<td>mA</td>
<td>IREG2=0mA</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>Reg.L1</td>
<td>- 90 180</td>
<td>mV</td>
<td>VIN=5.5 to 25V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>Reg.L1</td>
<td>- 30 50</td>
<td>mV</td>
<td>IREG1=0 to 30mA</td>
</tr>
</tbody>
</table>

#### [3.3V linear regulator]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>REG2 output voltage</td>
<td>VREG2</td>
<td>3.27 3.30 3.33</td>
<td>V</td>
<td>IREG2=1mA</td>
</tr>
<tr>
<td>Maximum current</td>
<td>IREG2</td>
<td>100 - -</td>
<td>mA</td>
<td>IREG1=0mA</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>Reg.L2</td>
<td>- - 20</td>
<td>mV</td>
<td>VIN=5.5 to 25V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>Reg.L2</td>
<td>- - 30</td>
<td>mV</td>
<td>IREG2=0 to 30mA</td>
</tr>
</tbody>
</table>

#### [5V linear regulator](Vo1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input threshold voltage</td>
<td>REG1th</td>
<td>4.1 4.4 4.7</td>
<td>V</td>
<td>Vo1: Sweep up</td>
</tr>
<tr>
<td>Input delay time</td>
<td>TREG1</td>
<td>1.5 3.0 6.0</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Switch resistance</td>
<td>RREG1</td>
<td>- 1.0 3.0</td>
<td>Ω</td>
<td></td>
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</tbody>
</table>

#### [Under Voltage lock out block]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>REG1 threshold voltage</td>
<td>REG1_UVLO</td>
<td>3.9 4.2 4.5</td>
<td>V</td>
<td>REG1: Sweep up</td>
</tr>
<tr>
<td>Hysteresis voltage</td>
<td>dV_UVLO</td>
<td>50 100 200</td>
<td>mV</td>
<td>REG1, Sweep down</td>
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</table>

#### [Output voltage sense block]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback voltage1</td>
<td>VFB1</td>
<td>0.693 0.700 0.707</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FB1 bias current</td>
<td>IFB1</td>
<td>- 0 1</td>
<td>μA</td>
<td>FB1=REF</td>
</tr>
<tr>
<td>Output discharge resistance1</td>
<td>RDISOUT1</td>
<td>50 100 200</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Feedback voltage2</td>
<td>VFB2</td>
<td>0.693 0.700 0.707</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FB2 bias current</td>
<td>IFB2</td>
<td>- 0 1</td>
<td>μA</td>
<td>FB2=REF</td>
</tr>
<tr>
<td>Output discharge resistance2</td>
<td>RDISOUT2</td>
<td>50 100 200</td>
<td>Ω</td>
<td></td>
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</tbody>
</table>
### Electrical characteristics – Continued
(unless otherwise noted, $T_a=25^\circ C$, $V_IN=12V$, $CTL=OPEN$, $EN1=EN2=5V$, $FS1=FS2=51k\Omega$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN.</td>
<td>TYP.</td>
<td>MAX.</td>
</tr>
<tr>
<td>[H(^3)REG block]</td>
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<tr>
<td>On time 1</td>
<td>TON1</td>
<td>0.760</td>
<td>0.910</td>
<td>1.060</td>
</tr>
<tr>
<td>On time 2</td>
<td>TON2</td>
<td>0.470</td>
<td>0.620</td>
<td>0.770</td>
</tr>
<tr>
<td>Maximum On time 1</td>
<td>TONMAX1</td>
<td>2.5</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Maximum On time 2</td>
<td>TONMAX2</td>
<td>1.65</td>
<td>3.3</td>
<td>6.6</td>
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<tr>
<td>Minimum Off time</td>
<td>TOFFMIN</td>
<td>-</td>
<td>0.2</td>
<td>0.4</td>
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<tr>
<td>[FET driver block]</td>
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<td></td>
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<tr>
<td>HG higher side ON resistor</td>
<td>HGHON</td>
<td>-</td>
<td>3.0</td>
<td>6.0</td>
</tr>
<tr>
<td>HG lower side ON resistor</td>
<td>HGLON</td>
<td>-</td>
<td>2.0</td>
<td>4.0</td>
</tr>
<tr>
<td>LG higher side ON resistor</td>
<td>LGHON</td>
<td>-</td>
<td>2.0</td>
<td>4.0</td>
</tr>
<tr>
<td>LG lower side ON resistor</td>
<td>LGLON</td>
<td>-</td>
<td>0.5</td>
<td>1.0</td>
</tr>
<tr>
<td>[Over voltage protection block]</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>OVP threshold voltage</td>
<td>VOVP</td>
<td>0.77</td>
<td>0.84</td>
<td>0.91</td>
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<tr>
<td>OVP Hysteresis</td>
<td>dV_OVP</td>
<td>50</td>
<td>150</td>
<td>300</td>
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<tr>
<td>[Short circuit protection block]</td>
<td></td>
<td></td>
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<tr>
<td>SCP threshold voltage</td>
<td>VSCP</td>
<td>0.42</td>
<td>0.49</td>
<td>0.56</td>
</tr>
<tr>
<td>Delay time</td>
<td>TSCP</td>
<td>0.4</td>
<td>0.75</td>
<td>1.5</td>
</tr>
<tr>
<td>[Current limit protection block]</td>
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</tr>
<tr>
<td>Offset voltage</td>
<td>dVSMAX</td>
<td>80</td>
<td>100</td>
<td>120</td>
</tr>
<tr>
<td>[Power good block]</td>
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</tr>
<tr>
<td>Power good low threshold</td>
<td>VPGTHL</td>
<td>0.525</td>
<td>0.595</td>
<td>0.665</td>
</tr>
<tr>
<td>Power good low voltage</td>
<td>VPGL</td>
<td>-</td>
<td>0.1</td>
<td>0.2</td>
</tr>
<tr>
<td>Delay time</td>
<td>TPGOOD</td>
<td>0.4</td>
<td>0.75</td>
<td>1.5</td>
</tr>
<tr>
<td>Power good leakage current</td>
<td>ILEAKPG</td>
<td>-2</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>[Soft start block]</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Charge current</td>
<td>ISS</td>
<td>1.5</td>
<td>2.3</td>
<td>3.1</td>
</tr>
<tr>
<td>Standby voltage</td>
<td>VSS_STB</td>
<td>-</td>
<td>-</td>
<td>50</td>
</tr>
<tr>
<td>[Mode control block]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCTL Low voltage</td>
<td>VMCTL_L</td>
<td>-0.3</td>
<td>-</td>
<td>0.3</td>
</tr>
<tr>
<td>MCTL High voltage</td>
<td>VMCTL_H</td>
<td>2.3</td>
<td>-</td>
<td>REG1 +0.3</td>
</tr>
<tr>
<td>MCTL bias current</td>
<td>IMCTL</td>
<td>8</td>
<td>16</td>
<td>24</td>
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</table>
### Output condition table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th>DC/DC1</th>
<th>DC/DC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTL</td>
<td>EN1</td>
<td>EN2</td>
<td>REG1(5V)</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>OFF</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>OFF</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>OFF</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>OFF</td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
<td>High</td>
<td>ON</td>
</tr>
<tr>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>ON</td>
</tr>
<tr>
<td>High</td>
<td>High</td>
<td>High</td>
<td>ON</td>
</tr>
</tbody>
</table>

※ CTL pin is connected to VIN pin with 1MΩ resistor (pull up) internal IC.
※ EN pin is connected to AGND pin with 1MΩ resistor (pull down) internal IC.

### Block Diagram, Application circuit

[Diagram of the application circuit]
**Pin Configuration**

- **Input Control Mode**
  - MCTL1: Low
  - MCTL2: Low
  - Control Mode: SLLM

- **Control Mode**
  - MCTL1: High
  - MCTL2: High
  - Control Mode: QLLM

  - MCTL1: High
  - MCTL2: Low
  - Control Mode: Forced Continuous Mode

  - MCTL1: High
  - MCTL2: High
  - Control Mode: Forced Continuous Mode

- **MCTL pin is connected to AGND pin with 500kΩ resistor (pull down) internal IC**

**Pin Function Table**

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>PIN name</th>
<th>PIN Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW2</td>
<td>Highside FET source pin 2</td>
</tr>
<tr>
<td>2</td>
<td>HG2</td>
<td>Highside FET gate drive pin 2</td>
</tr>
<tr>
<td>3</td>
<td>BOOT2</td>
<td>HG Driver power supply pin 2</td>
</tr>
<tr>
<td>4</td>
<td>EN2</td>
<td>Vo2 ON/OFF pin (High=ON, Low, OPEN=OFF)</td>
</tr>
<tr>
<td>5</td>
<td>PGOOD2</td>
<td>Vo2 Power Good Open Drain Output pin</td>
</tr>
<tr>
<td>6</td>
<td>SS2</td>
<td>Vo2 Soft start pin</td>
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<td>7</td>
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<td>Vo2 Output voltage sense pin</td>
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<td>8</td>
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<td>10</td>
<td>FS2</td>
<td>Input pin for setting Vo2 frequency</td>
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<tr>
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<td>Vo2 output voltage feedback pin</td>
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<td>13</td>
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<td>14</td>
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<td>15</td>
<td>FS1</td>
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<td>16</td>
<td>MCTL2</td>
<td>Mode switch pin 2 (OPEN = L)</td>
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<td>17</td>
<td>ILIM1</td>
<td>OCP setting pin 1</td>
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<tr>
<td>18</td>
<td>MCTL1</td>
<td>Mode switch pin 1 (OPEN = L)</td>
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<tr>
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<td>Lowside FET gate drive pin 1</td>
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<tr>
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<td>Vo1</td>
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<td>28</td>
<td>REG2</td>
<td>3.3V Linear regulator output pin</td>
</tr>
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<td>29</td>
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<td>5V Linear regulator output pin</td>
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<td>VIN</td>
<td>Power supply input pin</td>
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<td>31</td>
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<td>FIN</td>
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</tr>
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2010.03 - Rev.A
Electrical characteristic curves (Reference data)

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- **Fig.3 Switching Waveform**
  (Vo=5V, QLLM, Io=0A)

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- **Fig.9 Switching Waveform**
  (Vo=1V, PWM, Io=0A)

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Pin Descriptions

- **Vin (30 pin)**
  This is the main power supply pin. The input supply voltage range is 5.5V to 25V. The duty cycle of BD9528MUV is determined by input voltage and control output voltage. Therefore, when VIN voltage fluctuated, the output voltage also becomes unstable. Since VIN line is also the input voltage of switching regulator, stability depends on the impedance of the voltage supply. It is recommended to establish bypass capacitor and CR filter suitable for the actual application.

- **CTL (9 pin)**
  When CTL pin voltage is at least 2.3V, the status of the linear regulator output becomes active (REG1=5V, REG2=3.3V). Conversely, the status switches off when CTL pin voltage goes lower than 0.8V. The switching regulator doesn't become active when the status of CTL pin is low, if the status of EN pin is high.
  (CTL pin is connected to VIN pin with 1MΩ resistor(pull up) internal IC)

- **EN1, 2 (21 pin, 4 pin)**
  When EN pin voltage is at least 2.3V, the status of the switching regulator becomes active. Conversely, the status switches off when EN pin voltage goes lower than 0.8V.
  (EN pin is connected to AGND pin with 1MΩ resistor(pull down) internal IC)

- **REG1 (29 pin)**
  This is the output pin for 5V linear regulator and also active in power supply for driver and control circuit of the inside. The standby function for REG1 is determined by CTL pin. The voltage is 5V, with 100mA current ability. It is recommended that a 10μF capacitor (X5R or X7R) be established between REG1 and GND.

- **REG2 (28 pin)**
  This is the output pin for 3.3V linear regulator. The standby function for REG2 is determined by CTL. The voltage is 3.3V, with 50mA current ability. It is recommended that a 10μF capacitor (X5R or X7R) be established between REG2 and GND.

- **REF (12 pin)**
  This is the setting pin for output voltage of switching regulator. This IC controls the voltage in the status of REF≒FB.

- **FB 1, 2 (14 pin, 11 pin)**
  This is the feedback pin from the output of switching regulator. This IC controls the voltage in the status of REF≒FB.

- **Vo1 (27 pin)**
  This is the output discharge pin, and output voltage feedback pin for frequency setting. When the voltage is beyond 4.4V from the external power supply during operation, it supplies REG1.

- **Vo2 (7 pin)**
  This is the output discharge pin, and output voltage feedback pin for frequency setting.

- **SS1, 2 (19 pin, 6 pin)**
  This is the setting pin for soft start. The rising time is determined by the capacitor connected between SS and GND, and the fixed current inside IC after it is the status of low in standby mode. It controls the output voltage till SS voltage catch up the REF pin to become the SS terminal voltage.

- **FS1, 2 (15 pin, 10 pin)**
  This is the input pin for setting the frequency. It is available to set it in frequency range is 200KHz to 500kHz.

- **ILIM1, 2 (17 pin, 8 pin)**
  BD9528MUV detects voltage differential between SW and PGND, and set OCP. OCP setting current value is determined by the resistance value of ILIM pin. FET of various Ron is available.

- **PGOOD 1, 2 (20 pin, 5 pin)**
  This is the open drain pin for deciding the output of switching regulator.

- **MCTL1, 2 (18 pin, 16 pin)**
  This is the switching shift pin for SLLM (Simple Light Load Mode). MCTL pin is at low level when it goes lower than 0.8V, and at high level when it goes higher than 2.3V.
  (MCTL pin is connected to AGND pin with 500kΩ resistor(pull down) internal IC)

- **AGND (13 pin)**
  This is the ground pin.
• **BOOT1, 2 (22 pin, 3 pin)**
  This is the power supply pin for high side FET driver. The maximum voltage range to GND pin is to 35V, to SW pin is to 7V. In switching operations, the voltage swings from (VIN+REG1) to REG1 by BOOT pin operation.

• **HG1, 2 (23 pin, 2 pin)**
  This is the highside FET gate drive pin. It is operated in switching between BOOT to SW. In case the output MOS is 3ohm/the status of Hi, 20hm/the status of Low, it is operated hi-side FET gate in high speed.

• **SW1, 2 (24 pin, 1 pin)**
  This is the ground pin for high side FET drive. The maximum voltage range to GND pin is to 30V. Switching operation swings from the status of BOOT to the status of GND.

• **LG1, 2 (26 pin, 31 pin)**
  This is the lowside FET gate drive pin. It is operated in switching between REG1 to PGND. In case the output MOS is 2ohm/the status of Hi, 0.5ohm/the status of Low, it is operated low-side FET gate in high speed.

• **PGND1, 2 (25 pin, 32 pin)**
  This is the ground pin for low side FET drive.
Explanation of Operation

The BD9528MUV is a 2ch synchronous buck regulator controller incorporating ROHM's proprietary H^3REG CONTROLLA control system. Because controlling of output voltage by a comparator, high response is realized with not relying on the switching frequency. And, when VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the TON time interval. Thus, it serves to improve the regulator's transient response. Activating the Light Load Mode will also exercise Simple Light Load Mode (SLLM) control when the load is light, to further increase efficiency.

H^3Reg™ control

![H3Reg Diagram]

If VIN voltage drops because of the battery voltage fall, ontime TON and offtime TOFF is determined by the following formula:

\[ TON = \frac{VOUT}{VIN} \times \frac{1}{f} \] ・・・ (1)

If VIN still drops and TOff equals to tminoff (tminoff: Minimum OFF time, regulated inside IC), because Toff cannot shorten anymore, as a result output voltage drops. In H^3Reg™ system, lengthening TON time than regulated TON (lengthen TON time until FB > REF)
enables to operate stable not to drop the output voltage even if VIN turns to be low. With the reason above, it is suitable for 2-cell battery.

Light Load Control (SLLM)

In SLLM, when the status of LG is OFF and the coil current is within 0A (it flows to SW from VOUT.), SLLM function is operated to prevent output next HG. The status of HG is ON, when FB falls below reference voltage again.

In QLLM, when the status of LG is OFF and the coil current is within 0A (it flows to SW from VOUT.), QLLM function is operated to prevent output next HG. Then, FB falls below the output programmed voltage within the programmed time (typ=40μs), the status of HG is ON. In case FB doesn’t fall in the programmed time, the status of LG is ON forcibly and VOUT falls. As a result, the status of next HG is ON.

<table>
<thead>
<tr>
<th>MCTL1</th>
<th>MCTL2</th>
<th>Control mode</th>
<th>Running</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>SLLM</td>
<td>PWM</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>QLLM</td>
<td>PWM</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>PWM</td>
<td>PWM</td>
</tr>
</tbody>
</table>

Attention: H^Reg^TM CONTROLLA monitors the supplying current from capacitor to load, using the ESR of output capacitor, and realize the rapid response. Bypass capacitor used at each load (Ex. Ceramic capacitor) exerts the effect with connecting to each load side. Do not put a ceramic capacitor on COUT side of power supply.

Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage "ramping start." Soft start timing and incoming current are calculated with formulas (2) and (3) below.

Soft start time

\[
T_{ss} = \frac{\text{REF} \times \text{Css}}{2.3 \mu \text{A} \text{(typ)}} \quad \text{[sec]} \quad \cdots (2)
\]

Incoming current

\[
I_{in} = \frac{\text{CO} \times \text{VOUT}}{\text{Tss}} \quad \text{[A]} \quad \cdots (3)
\]

(Css: Soft start capacitor; CO: Output capacitor)
Notes when waking up with CTL pin or VIN pin

If EN pin is High or short (or pull up resistor) to REG1 pin, IC starts up by switching CTL pin, the IC might fail to start up (SCP function) with the reason below, please be careful of SS pin and REF pin capacitor capacity.

1. **Delay SCP**
   - PWM (Switching control signal) delay: 1ms (typ.)
2. **SCP circuit**
3. **BG**
4. **SCP_REF**
5. **SCP**
   - SCP turns ON and shuts down if REF voltage does not reach SCP_REF (0.49V)
6. **FB**
7. **REG1, REG2**
   - REG1 UVLO cancellation
8. **SS**
9. **CTRL (VIN)**
10. **REF**
   - REF start-up time < SS start-up time
11. **SCP function masked**
12. **SCP mask cancellation**
13. **FB starts up as SS reference**
14. **FB starts up as REF reference**

After the end of SS wake-up, within SCP delay time (1ms), if REF voltage does not reach SCP_REF (0.49V), SCP turns ON and shuts down.

**Inner reference circuit**

**SCP function masked**

SCP function is masked until SS pin reaches cramp voltage (2.5V).
● Output Discharge

It will be available to use if connecting VOUT pin to DC/DC output. (Total about 100Ω). Discharge function operates when ① EN='L'
② UVLO=ON (if input voltage is low) ③ SCP Latch time ④ TSD=ON. The function at output discharge time is shown as left.

(1) during EN='H' → 'L'
If EN pin voltage is below than EN threshold voltage, output discharge function is operated, and discharge output capacitor charge.

(2) during VIIN=CTL=H → 0V
① IC is in normal operation until REG1 voltage becomes lower than UVLO voltage. However, because VIN voltage also becomes low, output voltage will drop, too.
② If REG1 voltage reaches the UVLO voltage, output discharge function is operated, and discharge output capacitor charge.
③ In addition, if REG1 voltage drops, inner IC logic cannot operate, so that output discharge function does not work, and becomes output Hi-z. (In case, FB has resistor against GND, discharge at the resistor.)
• Timer Latch Type Short Circuit Protection

Short protection kicks in when output falls to or below REF × 0.7.
When the programmed time period elapses, output is latched OFF to prevent destruction of the IC. (HG=Low, LG=Low) Output voltage can be restored either by reconnecting the EN pin or disabling UVLO.

• Over Voltage Protection

When output rise to or above REF × 1.2 (typ), output over voltage protection is exercised, and low side FET goes up maximum for reducing output. (LG=High, HG=Low). When output falls, output voltage can be restored., and go back to the normal operation.

• Over current protection circuit

During the normal operation, when FB becomes less than REF, HG becomes High during the time tON, and after HG becomes OFF, it output LG.
However, when inductor current exceeds ILIMIT threshold, next HG pulse doesn’t pulsate until it is lower than ILIMIT level.
**External Component Selection**

1. **Inductor (L) selection**

   The inductor value is a major influence on the output ripple current. As formula (4) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

   \[ \Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \quad \cdots (4) \]

   The proper output ripple current setting is about 30% of maximum output current.

   \[ \Delta I_L = 0.3 \times I_{OUT\max} \quad [A] \quad \cdots (5) \]

   \[ L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [H] \quad \cdots (6) \]

   (\( \Delta I_L \): output ripple current; \( f \): switch frequency)

   ※Passing a current larger than the inductor’s rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor rated current value.

   ※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2. **Output Capacitor (Co) Selection**

   When determining the proper output capacitor, be sure to factor in the equivalent series resistance required to smooth output ripple and maintain a stable output voltage range.

   Output ripple voltage is determined as in formula (7) below.

   \[ \Delta V_{OUT} = \Delta I_L \times ESR \times ESL \times \Delta I_L / T_{ON} \quad \cdots (7) \]

   (\( \Delta I_L \): Output ripple current; \( ESR \): \( Co \) equivalent series resistance)

   ※In selecting a capacitor, make sure the capacitor rating allows sufficient margin relative to output voltage. Note that a lower ESR can minimize output ripple voltage.

   Please give due consideration to the conditions in formula (8) below for output capacity, bear in mind that output rise time must be established within the soft start time frame. Capacitor for bypass capacitor is connected to Load side which connect to output in output capacitor capacity (\( C_{EXT} \), figure above). Please set the soft start time or over current detecting value, regarding these capacities.

   \[ C_o \leq \frac{T_{ss} \times \text{Limit-I}_{OUT}}{V_{OUT}} \quad \cdots (8) \]

   T_{ss}: Soft start time

   Limit: Over current detection

   Note: Improper capacitor may cause startup malfunctions.

3. **Input Capacitor (Cin) Selection**

   The input capacitor selected must have low enough ESR resistance to fully support large ripple output, in order to prevent extreme over current. The formula for ripple current IRMS is given in (9) below.

   \[ IRMS = I_{OUT} \times \sqrt{\frac{V_{IN}(V_{IN}-V_{OUT})}{V_{IN}}} \quad [A] \quad \cdots (9) \]

   Where \( V_{IN}=2 \times V_{OUT} \), \( IRMS = \frac{I_{OUT}}{2} \)

   A low ESR capacitor is recommended to reduce ESR loss and maximize efficiency.
4. MOSFET Selection

MOSFET may cause the loss as below, so please select proper FET for each.

\[ P_{\text{main}} = PRON + PGATE + PTRAN \]

\[ P_{\text{main}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times R_{\text{ON}} \times I_{\text{OUT}}^2 + C_{\text{iss}} \times f \times V_{\text{DD}} + \frac{V_{\text{IN}}^2 \times C_{\text{rss}} \times I_{\text{OUT}} \times f}{I_{\text{DRIVE}}} \] \hspace{1cm} (10)

(Ron: On-resistance of FET, Ciss: FET gate capacitance; f: Switching frequency Crss: FET inverse transfer function; Idrive: Gate peak current)

\[ P_{\text{syn}} = PRON + PGATE \]

\[ P_{\text{syn}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}}} \times R_{\text{ON}} \times I_{\text{OUT}}^2 + C_{\text{iss}} \times f \times V_{\text{DD}} \] \hspace{1cm} (11)

5. Setting output voltage

This IC is operated that output voltage is \( V_{\text{REF}} = V_{\text{FB}} \).

And it is operated that output voltage is feed back to FB pin.

\[ \Delta V_{\text{OUT}} = \Delta V_{\text{ripple}} \times ESR \]

\[ \Delta V_{\text{ripple}} = (V_{\text{IN}} - V_{\text{OUT}}) \times \frac{V_{\text{OUT}}}{(L \times V_{\text{IN}} \times f)} \]

※(Notice) Please set \( \Delta V_{\text{OUT}} \) more than 20mV

Ex. \( V_{\text{IN}} = 20V, V_{\text{OUT}} = 5V, f = 300kHz, L = 2.5uH, ESR = 20m\Omega, R1 = 56K\Omega, R2 = 9.1k\Omega \)

\( \Delta V_{\text{ripple}} = (20V - 5V) \times 5V / (2.5 \times 10^{-6}H \times 20V \times 300 \times 10^3Hz) = 5[A] \)

\( \Delta V_{\text{OUT}} = 5A \times 20 \times 10^{-3}\Omega = 0.1[V] \)

\( V_{\text{OUT}} = (51k\Omega + 9.1k\Omega) / 9.1k\Omega + 1/2 \times 0.1V = 5.057[V] \)

Select (R1 + R2) under 100K\Omega (recommend)
6. Setting over current protection

Detecting the ON resistance (between SW and PGND voltage) of MOSFET at low side, it sets the over current voltage protection.

Over current reference voltage \( \text{ILIM}_{\text{ref}} \) is determined as in formula (12) below.

\[
\text{ILIM}_{\text{ref}} = \frac{10 \times 10^2}{R_{\text{ILIM}}[k\Omega] \times R_{\text{ON}}[m\Omega]} \quad [A] \ldots (12)
\]

\( R_{\text{ILIM}} \): Resistance for setting of over current voltage protection value[k\Omega]
\( R_{\text{ON}} \): Low side ON resistance value of FET[m\Omega]

However, the value, which sets the over current protection actually, is determined by the formula (13) below.

\[
I_{\text{loop}} = \text{ILIM}_{\text{ref}} + \frac{1}{2} \cdot \Delta I_L
\]

\[
= \text{ILIM}_{\text{ref}} + \frac{1}{2} \times \frac{\text{VIN} - \text{Vo}}{\text{L}} \times \frac{1}{\text{f}} \times \frac{\text{Vo}}{\text{VIN}} \quad \ldots (13)
\]

\( \Delta I_L \): Coil ripple current[A], \( \text{VIN} \): Input voltage[V], \( \text{Vo} \): Output voltage[V], \( \text{f} \): Switching frequency[Hz], \( \text{L} \): Coil inductance[H]

(Example)

If load current 5A want to be realized with \( \text{VIN}=6 \sim 19V \), \( \text{VOUT}=5V \), \( \text{f}=400kHz \), \( \text{L}=2.5uH \), \( R_{\text{ON}}=20m\Omega \), the formula would be below.

\[
I_{\text{loop}} = \frac{10k}{R_{\text{ILIM}}[k\Omega] \times R_{\text{ON}}[m\Omega]} + \frac{1}{2} \times \frac{\text{VIN} - \text{Vo}}{\text{L}} \times \frac{1}{\text{f}} \times \frac{\text{Vo}}{\text{VIN}} > 5
\]

When \( \text{VIN}=6V \), \( I_{\text{loop}} \) will be minimum (this is because the ripple current is also minimum) so that if each condition is input, the formula will be the following: \( R_{\text{ILIM}}<109.1[k\Omega] \).

※To design the actual board, please consider enough margin for FET ON resistor dispersion, coil inductor dispersion, IC over current reference value dispersion, frequency dispersion.

7. Relation between output voltage and TON time

The BD9528MUV, both 1ch and 2ch, are high efficiency synchronous regulator controller with frequency variable.

TON time varies with Input voltage [VIN], output voltage [VOUT], and RFS of FS pin resistance.

TON time is calculated with the following formula:

\[
\text{TON} = k \cdot \frac{\text{VOUT} \times \text{RFS}}{\text{VIN}} \quad [\text{nsec}] \ldots (14)
\]

From TON time above, frequency on application condition is following:

\[
\text{Frequency} = \frac{\text{VOUT}}{\text{VIN}} \times \frac{1}{\text{TON}} \quad [\text{kHz}] \ldots (15)
\]

However, real-life considerations (such as the external MOSFET gate capacitor and switching speed) must be factored in as they affect the overall switching rise and fall time, so please confirm in reality by the instrument.
8. Relation between output voltage and frequency

Because the BD9528MUV is TON time focused regulator controller, if output current is up, switching loss of Coil, MOSFET and output capacitor will increase, and frequency will be fast.

Loss of each Coil, MOSFET and output capacitor are below.

\[
\begin{align*}
1. & \text{ Coil loss } = I_{OUT}^2 \times DCR \\
2. & \text{ MOSFET (High Side) loss } = I_{OUT}^2 \times R_{ONh} \times \frac{V_{OUT}}{V_{IN}} \\
3. & \text{ MOSFET (Low Side) loss } = I_{OUT}^2 \times R_{ONl} \times (1- \frac{V_{OUT}}{V_{IN}})
\end{align*}
\]

(Ronh : ON resistance of high side MOSFET, Ronl : ON resistance of low side MOSFET, ESR : Output capacitor equivalent cascade resistance)

Regarding those loss above and frequency formula, it is determined below.

\[
T (=1/Freq) = \frac{V_{IN} \times I_{OUT} \times T_{ON}}{V_{OUT} \times I_{OUT} + 1 + 2 + 3} \quad \cdots (16)
\]

However, real-life considerations (such as parasitic resistance element of Layout pattern) must be factored in as they affect the loss, please confirm in reality by the instrument.
● I/O Equivalent Circuit

1, 24pin (SW2, SW1)  
2, 23pin (HG2, HG1)  
3, 22pin (BOOT2, BOOT1)  
4, 21pin (EN2, EN1)  
5, 20pin (PGOOD2, PGOOD1)  
6, 19pin (SS2, SS1)  
12pin (REF)  
11, 14pin (FB2, FB1)  
10, 15pin (FS2, FS1)  
16, 18pin (MCTL2, MCTL1)  
9pin (CTL)  
26, 31pin (LG1, LG2)
### I/O Equivalent Circuit

<table>
<thead>
<tr>
<th>7, 27pin (Vo2, Vo1)</th>
<th>28pin (REG2)</th>
<th>29pin (REG1)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Circuit Diagram" /></td>
<td><img src="image2.png" alt="Circuit Diagram" /></td>
<td><img src="image3.png" alt="Circuit Diagram" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>30pin (VIN)</th>
<th>8, 17pin (ILIM2, ILIM1)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image4.png" alt="Circuit Diagram" /></td>
<td><img src="image5.png" alt="Circuit Diagram" /></td>
</tr>
</tbody>
</table>
Evaluation Board Circuit (Vo1=5V/8A f1=300kHz Vo2=3.3V/8A f2=300kHz)

DESIGNATION | RATING | PART No. | COMPANY
--- | --- | --- | ---
R1 | 0Ω | - | -
R2 | - | - | -
R3 | 0Ω | - | -
R4 | 0Ω | - | -
R5 | 68kΩ | MCR03 | ROHM
R6 | 68kΩ | MCR03 | ROHM
R7 | 75kΩ | MCR03 | ROHM
R8 | 75kΩ | MCR03 | ROHM
R9 | 0Ω | - | -
R10 | 0Ω | - | -
R11 | 0Ω | - | -
R12 | 0Ω | - | -
R13 | 0Ω | - | -
R14 | 0Ω | - | -
R15 | 100kΩ | MCR03 | ROHM
R16 | 100kΩ | MCR03 | ROHM
R17 | 91kΩ | MCR03 | ROHM
R18 | 15kΩ | MCR03 | ROHM
R19 | 30kΩ | MCR03 | ROHM
R20 | 8.2kΩ | MCR03 | ROHM
R27 | 0Ω | - | -
R28 | 0Ω | - | -
C1 | 10μF (25V) | CM32XR106M25A | KYOCERA
C2 | 10μF (6.3V) | GRM21BB10J106KD | MURATA
C3 | 10μF (6.3V) | GRM21BB10J106KD | MURATA
C4 | 0.1μF (6.3V) | GRM21BB10J104KD | MURATA
C5 | 2200μF (50V) | GRM188B11H102KD | MURATA
C6 | 2200μF (50V) | GRM188B11H102KD | MURATA
C7 | 0.47μF (10V) | GRM188B11A474KD | MURATA
C8 | 0.47μF (10V) | GRM188B11A474KD | MURATA
C9 | 10μF (25V) | CM32XR710625A | KOCERA
C10 | 10μF (25V) | CM32XR710625A | KYOCERA
C11 | 330μF | 6TPE330MI | SANYO
C12 | - | - | -
C13 | - | - | -
C14 | - | - | -
C15 | - | - | -
C16 | - | - | -
C17 | - | - | -
C18 | 330μF | 6TPE330MI | SANYO
C19 | - | - | -
C20 | - | - | -
C21 | - | - | -
C22 | - | - | -
C23 | - | - | -
C24 | - | - | -
C25 | - | - | -
C26 | - | - | -
D1 | Diode | RSX501L-20 | ROHM
D2 | Diode | RSX501L-20 | ROHM
L1 | 2.5μH | CDEP105NP-2R5MC-32 | Sumida
L2 | 2.5μH | CDEP105NP-2R5MC-32 | Sumida
Q1 | FET | uPA2709 | NEC
Q2 | FET | uPA2709 | NEC
Q3 | FET | uPA2709 | NEC
Q4 | FET | uPA2709 | NEC
U1 | - | BD9528MUV | ROHM
Evaluation Board Circuit for Low input voltage
(Vo1=5V/8A f1=300kHz Vo2=3.3V/8A f2=300kHz)

DESIGNATION | RATING | PART No. | COMPANY
---|---|---|---
R1 | 0Ω | - | -
R2 | 0Ω | - | -
R3 | 0Ω | - | -
R4 | 0Ω | - | -
R5 | 68kΩ | MCR03 | ROHM
R6 | 68kΩ | MCR03 | ROHM
R7 | 75kΩ | MCR03 | ROHM
R8 | 75kΩ | MCR03 | ROHM
R9 | 0Ω | - | -
R10 | 10Ω | - | -
R11 | 10Ω | - | -
R12 | 0Ω | - | -
R13 | 10Ω | - | -
R14 | 10Ω | - | -
R15 | 100kΩ | MCR03 | ROHM
R16 | 100kΩ | MCR03 | ROHM
R17 | 56kΩ | MCR03 | ROHM
R18 | 9.1kΩ | MCR03 | ROHM
R19 | 30kΩ | MCR03 | ROHM
R20 | 8.2kΩ | MCR03 | ROHM
R27 | 0Ω | - | -
R28 | 0Ω | - | -
C1 | 10uF(25V) | CM32XR7106M25A | KYOCERA
C2 | 10uF(6.3V) | GRM21BB10J106KD | MURATA
C3 | 10uF(6.3V) | GRM21BB10J106KD | MURATA
C4 | 0.1uF(6.3V) | GRM21BB10J104KD | MURATA
C5 | 2200pF(50V) | GRM188B11H102KD | MURATA
C6 | 2200pF(50V) | GRM188B11H102KD | MURATA
C7 | 0.47uF(10V) | GRM188B11A474KD | MURATA
C8 | 0.47uF(10V) | GRM188B11A474KD | MURATA
C9 | 10uF(25V) | CM32XR7106M25A | KYOCERA
C10 | 10uF(25V) | CM32XR7106M25A | KYOCERA
C11 | 330uF | 6TPB330ML | SANYO
C12 | - | - | -
C13 | - | - | -
C14 | - | - | -
C15 | - | - | -
C16 | - | - | -
C17 | - | - | -
C18 | 330uF | 6TPE330ML | SANYO
C19 | - | - | -
C20 | - | - | -
C21 | - | - | -
C22 | - | - | -
C23 | 10pF(50V) | - | -
C24 | - | - | -
C25 | - | - | -
C26 | - | - | -
D1 | Diode | RSX501L-20 | ROHM
D2 | Diode | RSX501L-20 | ROHM
L1 | 2.5uH | CDEP105NP-2R5MC-32 | Sumida
L2 | 2.5uH | CDEP105NP-2R5MC-32 | Sumida
Q1 | FET | uPA2709 | NEC
Q2 | FET | uPA2709 | NEC
Q3 | FET | uPA2709 | NEC
Q4 | FET | uPA2709 | NEC
U1 | - | BD9528MUV | ROHM
● Handling method of unused pin during using only DC/DC 1ch

If using only 1ch DC/DC and 2ch pin is set to be off at all times, please manage the unused pin as diagram below.

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>PIN name</th>
<th>Management</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW2</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>HG2</td>
<td>Open</td>
</tr>
<tr>
<td>3</td>
<td>BOOT2</td>
<td>Open</td>
</tr>
<tr>
<td>4</td>
<td>EN2</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>PGOOD2</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>SS2</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>Vo2</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>ILIM1</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>FB2</td>
<td>GND</td>
</tr>
<tr>
<td>11</td>
<td>FS2</td>
<td>GND</td>
</tr>
<tr>
<td>31</td>
<td>LG2</td>
<td>Open</td>
</tr>
</tbody>
</table>
● Example of PCB layout

① Because high pulse current rush into power loop, consisted of input capacitor Cin, Output inductor L, and Output capacitor Co, this part layout should be built, including GND pattern, at parts side (upper side). Also, please avoid to draw via formation in power loop line. (The reason is that it will be a factor of noise because via oneself holds some nH parasitic inductance)

② FB pin has comparatively high impedance, so floating capacity should be minimum as possible. And feedback wiring from output should be taken properly, and put on shield, not going through around L (because of magnetic). Please be careful in drawing.

③ Trace from SW node pin to inductor should be cut short. And both inductor element pattern should be kept away. (Closer wiring has SW node noise influence Vo by parasitic capacity between wiring). This layout example shows that SW node is outside, but if the application board will be like that, SW node should be shielding, and consider the influence to other circuit.

④ Input capacitor Cin should be placed close to IC with low inductance and low impedance. If that is difficult, please place a capacitor for high frequency removal with PKG size small like 0.1uF (ESL small).

⑤ 2 layer and 3 layer are plain GND, so connect from parts side GND to plain GND by low impedance with many via as possible. Inner GND is only for shielding, so that not to form loop for high current.

⑥ Please take GND pattern space widely, and design layout to be able to increase radiation efficiency.

⑦ FS pin nad ILIM pin has high impedance. External resistor should be connected to "Silent GND".

---

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Input current A
Vin
Power GND
DC/DC
H3Reg controller
Inductor current
SW pin voltage
Vout
Power GND
Analog GND
Output current GND
Output current GND
GND
Input current B

Charger current
Cin

Current leveled
By capacitor
Input current A

Pulsed current flows by
ON/OFF of the switch
Input current B

Noise output!!
This part is shortened.

SW pin voltage

Vin

0V
SW pin voltage

Inductor ripple current

Inductor current

The noise has decreased
by LC filter

Output current

www.DataSheet.co.kr
www.DataSheet.co.kr

www.DataSheet4U.net
www.DataSheet4U.net
The influence of inductor is noted

The impedance of the output is low
= It may be long

The impedance of this line is high

This distance is shorted as much as possible

The impedance of FB pin is higher

Good layout

Bad layout
Notes for use

1. This integrated circuit is a monolithic IC, which (as shown in the figure below), has P+ isolation in the P substrate and between the various pins. A P-N junction is formed from this P layer and N layer of each pin, with the type of junction depending on the relation between each potential, as follows:
   - When GND > element A > element B, the P-N junction is a diode.
   - When element B > GND > element A, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, as well as operating malfunctions and physical damage. Therefore, be careful to avoid methods by which parasitic diodes operate, such as applying a voltage lower than the GND (P substrate) voltage to an input pin.

2. In some modes of operation, power supply voltage and pin voltage are reversed, giving rise to possible internal circuit damage. For example, when the external capacitor is charged, the electric charge can cause a VCC short circuit to the GND. In order to avoid these problems, inserting a VCC series countercurrent prevention diode or bypass diode between the various pins and the VCC is recommended.

3. Absolute maximum rating
   Although the quality of this IC is rigorously controlled, the IC may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because short mode or open mode cannot be specified when the IC is destroyed, it is important to take physical safety measures such as fusing if a special mode in excess of absolute rating limits is to be implemented.

4. GND potential
   Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.

5. Thermal design
   In order to build sufficient margin into the thermal design, give proper consideration to the allowable loss (Power Dissipation) in actual operation.

6. Short-circuits between pins and incorrect mounting position
   When mounting the IC onto the circuit board, be extremely careful about the orientation and position of the IC. The IC may be destroyed if it is incorrectly positioned for mounting. Do not short-circuit between any output pin and supply pin or ground, or between the output pins themselves. Accidental attachment of small objects on these pins will cause shorts and may damage the IC.

7. Operation in strong electromagnetic fields
   Use in strong electromagnetic fields may cause malfunctions. Use extreme caution with electromagnetic fields.
8. Thermal shutdown circuit
This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the operating temperature reaches 175°C (standard value), and has a hysteresis range of -15°C (standard value). When the IC chip temperature rises to the threshold, all the inputs automatically turn OFF. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

9. Capacitor between output and GND
When a larger capacitor is connected between the output and GND, Vcc or VIN shorted with the GND or 0V line – for any reason – may cause the charged capacitor current to flow to the output, possibly destroying the IC. Do not connect a capacitor larger than 1000uF between the output and GND.

10. Precautions for board inspection
Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

11. GND wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

● Thermal Derating Curve
© VQFN032V5050

![Thermal Derating Curve](image-url)
### Ordering part number

<table>
<thead>
<tr>
<th>B</th>
<th>D</th>
<th>9</th>
<th>5</th>
<th>2</th>
<th>8</th>
<th>M</th>
<th>U</th>
<th>V</th>
<th>-</th>
<th>E</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>Part No.</td>
<td>Package</td>
<td>MUV: VQFN032V5050</td>
<td>Packaging and forming specification</td>
<td>E2: Embossed tape and reel</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### VQFN032V5050

![VQFN032V5050 Diagram](image)

#### <Tape and Reel information>

<table>
<thead>
<tr>
<th>Tape</th>
<th>Embossed carrier tape</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
<td>2500pcs</td>
</tr>
<tr>
<td>Direction of feed</td>
<td>E2</td>
</tr>
</tbody>
</table>

- The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand.

- Order quantity needs to be multiple of the minimum quantity.

![Reel Diagram](image)
Notes

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